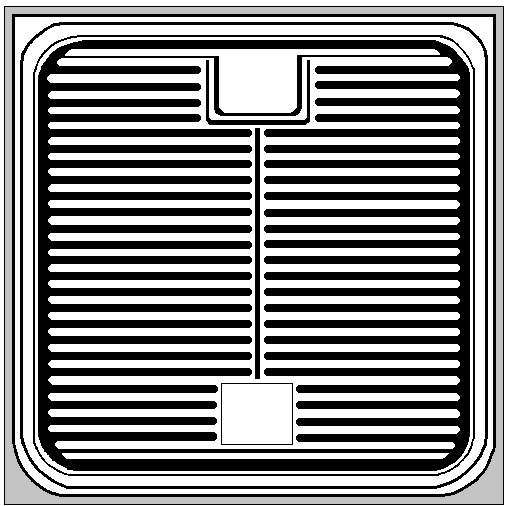
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**SOURCE**

**GATE**

**.042”**

**.042”**

**Chip back is Drain**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .005” X .005”**

**Backside Potential: Drain**

**Geometry: G17**

**APPROVED BY:DK DIE SIZE .042” X .042” DATE: 8/25/21**

**MFG: ZETEX THICKNESS: .010” P/N:ZVNL120C**

**DG 10.1.2**

#### Rev B, 7/19/02